WHAT IS CLAIMED IS:

1. A computer-implemented design method of a logic circuit comprising:

converting an algorithm of the logic circuit from an operation description having operators into a data flow graph having operation nodes executing the operators arranged in order of the executing;

allocating execution steps in the data flow graph, and inserting registers storing output data from the operation nodes after execution of the execution steps;

producing a data path of the logic circuit having operation units which served as the operation nodes and storage elements which served as the registers, and control information on the data path; and

producing an operator/operation unit database configured to retrieve the operation units executing the operators from the operators and configured to retrieve the operators outputting data stored in the registers which served as the storage elements from the execution steps and the storage elements.

2. The computer-implemented design method of a logic circuit as claimed in claim 1, further comprising:

producing a node/operator database configured to retrieve the operators executed at the operation nodes from the operation nodes based on the operation description and

the data flow graph and configured to retrieve the operators executed at the operation nodes outputting data stored in the registers from the registers; and

producing a node/operation unit database configured to retrieve the operation unit which served as the operation node from the operation nodes based on the data flow graph and the data path and configured to retrieve the registers which served as the storage elements from the execution step and the storage elements;

wherein the operator/operation unit database is produced based on the node/operator database and the node/operation unit database.

3. The computer-implemented design method of a logic circuit as claimed in claim 1, further comprising:

producing a register transfer level description of the logic circuit based on the data path and the control information;

substituting input data into the operation description, and calculating output data from the operators;

substituting the input data into the register transfer level description, and calculating storage data stored in the storage elements in the execution step;

retrieving the operators from the execution step and the storage elements of the calculated storage data based on the operator/operation unit database; and

determining whether the output data from the operators

and the storage data are the same as or different from each other.

4. The computer-implemented design method of a logic circuit as claimed in claim 1, further comprising:

retrieving the operation unit from the operators based on the operator/operation unit database.

5. A computer program product to be executed by a computer for designing a logic circuit, the computer program product comprising:

instructions configured to convert an algorithm of the logic circuit from an operation description having operators into a data flow graph having operation nodes executing the operators arranged in order of the executing;

instructions configured to allocate execution steps in the data flow graph, and inserting registers storing output data from the operation nodes after execution of the execution steps;

instructions configured to produce a data path of the logic circuit having operation units which served as the operation nodes and storage elements which served as the registers, and control information on the data path; and

instructions configured to produce an operator/operation unit database configured to retrieve the operation units executing the operators from the operators and to retrieve the operators outputting data stored in the registers which served as the storage elements from the

execution steps and the storage elements.

6. The computer program product to be executed by a computer as claimed in claim 5, further comprising:

instructions configured to produce a node/operator database configured to retrieve the operators executed at the operation nodes from the operation nodes based on the operation description and the data flow graph and to retrieve the operators executed at the operation nodes outputting data stored in the registers from the registers; and

instructions configured to produce a node/operation unit database configured to retrieve the operation unit which served as the operation nodes from the operation nodes based on the data flow graph and the data path and to retrieve the registers which served as the storage elements from the execution step and the storage elements;

wherein the operator/operation unit database is produced based on the node/operator database and the node/operation unit database.

7. The computer program product to be executed by a computer as claimed in claim 5, further comprising:

instructions configured to produce a register transfer level description of the logic circuit based on the data path and the control information;

instructions configured to substitute input data into the operation description, and to calculate output data from

the operators;

instructions configured to substitute the input data into the register transfer level description, and to calculate storage data stored in the storage elements in the execution step;

instructions configured to retrieve the operators from the execution step and the storage elements of the calculated storage data based on the operator/operation unit database; and

instructions configured to determine whether the output data from the operators and the storage data are the same as or different from each other.

8. The computer program product to be executed by a computer as claimed in claim 5, further comprising:

instructions configured to retrieve the operation unit from the operators based on the operator/operation unit database.

9. An apparatus for designing a logic circuit comprising:

a syntax analyzing unit configured to convert an algorithm of the logic circuit from an operation description having operators into a data flow graph having operation nodes executing the operators arranged in order of the executing;

a scheduling unit configured to allocate execution steps in the data flow graph, and inserting registers storing output data from the operation nodes after execution

of the execution steps;

a hardware allocating unit configured to produce a data path of the logic circuit having operation units which served as the operation nodes and storage elements which served as the registers, and control information on the data path; and

a correspondence information analyzing unit configured to produce an operator/operation unit database configured to retrieve the operation units executing the operators from the operators and to retrieve the operators outputting data stored in the registers served as the storage elements from the execution steps and the storage elements.

10. The apparatus for designing a logic circuit as claimed in claim 9, further comprising:

a node/operator correspondence information analyzing unit configured to produce a node/operator database configured to retrieve the operators executed at the operation nodes from the operation nodes based on the operation description and the data flow graph and to retrieve the operators executed at the operation nodes outputting data stored in the registers from the registers; and

a node/operation unit correspondence information analyzing unit configured to produce a node/operation unit database configured to retrieve the operation unit which served as the operation nodes from the operation nodes based

on the data flow graph and the data path and to retrieve the registers which served as the storage elements from the execution step and the storage elements;

wherein the operator/operation unit database is produced based on the node/operator database and the node/operation unit database.

11. The apparatus for designing a logic circuit as claimed in claim 9, further comprising:

a register transfer level description producing unit configured to produce a register transfer level description of the logic circuit based on the data path and the control information;

an operation description simulating unit configured to substitute input data into the operation description, and to calculate output data from the operators;

a register transfer level simulating unit configured to substitute the input data into the register transfer level description, and to calculate storage data stored in the storage elements in the execution step;

an operator retriever configured to retrieve the operators from the execution step and the storage elements of the calculated storage data based on the operator/operation unit database; and

a storage data determiner configured to determine whether the output data from the operators and the storage data are the same as or different from each other.

12. The apparatus for designing a logic circuit as claimed in claim 9, further comprising:

an operation unit retriever configured to retrieve the operation unit from the operators based on the operator/operation unit database.